REMARKS

Favorable reconsideration of this application in view of the foregoing amendments and remarks to follow are respectfully requested. Since the present response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested.

Prior to discussing the prior art rejections, Applicants take this opportunity to set forth the following brief remarks about the claimed invention. Applicants' invention utilizes a stacked gate structure to control the stress produced in the channel of the device, wherein the stacked gate structures includes a gate dielectric, a first stressed film layer of large grain size Si or SiGe formed on top of a gate dielectric layer, and a second stressed film layer of strained SiGe or strained Si:C formed on top the first stressed film layer, as recited in Claim 1. As required by Claim 1, Applicants' claimed gate structure produces stresses in the channel of the device. The applied references fail to teach or suggest at least these required features of Applicants' claims.

In the present Official Action, Claims 1 and 2 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2004/0195624A1 to Liu et al. ("Liu et al."). Claims 3-13 stand rejected, under 35 U.S.C. 103(a), as allegedly being unpatentable over Liu et al. in view of U.S. Patent Application Publication No. 2005/0189589 to Zhu et al. ("Zhu et al."). Applicants respectfully disagree and submit the following.

Turning first to the §102 rejection of Claims 1 and 2, Applicants note that Liu et al. fail to disclose a stacked gate structure of SiGe and/or Si:C that produces stress in the channel region of the transistor device positioned beneath the stacked gate structure of SSi(strained Si)/SiGe or SSi/Si:C, as recited in Claim 1. Applicants note that there is no suggestion throughout the Liu et al. disclosure of a gate region of stacked gate conductors or teaching of where a stacked gate

region produces a stress in the channel of a transistor device. Liu et al. merely teaches a gate composed of single gate conductor (see reference number 4 in Figure 1), wherein the single gate conductor is separated from the channel (see reference number 2 in Figure 1) by a gate dielectric (see reference number in Figure 1).

Referring to Page 2 of the Final Rejection, the Examiner alleges that Figures 1-3 of the Liu et al. disclosure meet the limitation of Applicants' claimed gate structure and alleges that Figures 1-3 depict a stacked gate region including SiGe, strained Si, oxide layer and polysilicon gate. Applicants respectfully disagree.

Applicants submit that the SiGe and strained Si that is being referred to by the Examiner in the rejection of Claims 1-2 under § 102 (e) is a strained Si fin 2 , which is not a gate structure and is in fact the channel of the finFET. A channel separates the source from the drain of the field effect transistor. Referring to paragraph 0002 of the Liu et al. disclosure, Liu et al. disclose that an advantage of a finFet is that the "Fin" can be so narrow that the whole Fin area is controlled by the gate and that when the finFET is turned off, there is no path through the Fin for carriers to move from source to drain. Referring to paragraph 0046, Liu et al. further describe the Fin (channel) of the device as follows:

> "As shown in Figure 1, the conventional Fin Si is substituted by novel strained Si structure. Referring to FIG. 2, the numerals 13 and 16 represent the thicknesses (T_1 and T_4) of the silicon layers 9 and 12, respectively, the numerals 14 and 15 represent the widths (T_2 and T_3) of the silicon layers 10 and 11, respectively, and the numerals 17 and 18 represent the height (H) and the width (W) of the SiGe embedded body 8, respectively. When the height (H) 17 and the width (W) 18 of the SiGe embedded body are much larger than the thickness of the Si layer (T_1) 13 thereunder, the SiGe embedded body is relaxed and the surrounding Si is strained. Because mobility of strained Si is very high, operating speed of the strained Si FinFET is fast."

Liu et al. utilize layers of SiGe and silicon within the Fin region, which is the channel of the device, to produce a strain in the channel. Liu et al. fail to teach or suggest a stacked structure including a first stressed film layer of large grain size Si or SiGe formed on top of a gate dielectric layer, and a second stressed film layer of strained SiGe or strained Si:C formed on top the first stressed film layer, and that the stacked gate structure of SiGe and/or Si:C produces stresses in the channel region of the transistor, as required by Claim 1.

Therefore, since Liu et al. fail to disclose each and every limitation of Claim 1, Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested. Furthermore, the § 102(e) rejection of Claim 2 is improper since each of these claims depend from Claim 1, which is not anticipated by Liu et al.

Turning to the §103 rejection of Claims 3-13, Applicants submit that Zhu et al. is disqualified as a reference. The statute under 35 U.S.C. §103(c) states that:

> Subject matter developed by another person, which qualifies as prior art only under one or more subjections (e), (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Applicants submit that the Zhu et al. reference was applied by the Examiner as prior art under 35 U.S.C. §103 via 35 U.S.C. §102(e). Applicants note in this regard that MPEP §706.02(k) states that:

> Effective November 29, 1999, subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person."

In view of the above, and the fact the present application and Zhu et al. "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person", the Zhu et al. reference is disqualified as a reference under 35 U.S.C. §103(c).

To evidence that the instant application and Zhu et al. "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person", the assignment document of the present application (recordation date April 23, 2004 at Reel 014525, Frame 0620) was compared with the recorded assignment of Zhu et al. (recordation date February 27, 2004 at Reel 014371, Frame 0604). In both instances, the inventors conveyed their entire interest to International Business Machines Corporation; therefore establishing common ownership between the instant application and the applied Zhu et al.

In view of the above information, Zhu et al. is disqualified as art and the instant §103 rejection is also solely based on Liu et al. Applicants submit, in this regard, that Liu et al. by itself does not anticipate, or render obvious, the claimed invention as discussed above. Thus, the rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

In view of the foregoing, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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